II B. Tech II Sem – Semester End Examinations – Supplementary – Feb 2023

**Subject Name: Computer Organization Subject Code: 194GA05404**

**Name & Signature of the Examiner: M. Narasimhulu**

**Scheme of Evaluation**

**SRIT R19**

**AY: 2022-23**

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|  | **PART-A** |  |
| 1a) | Memory unit is a component of a computer system. It is used to store data, instructions and information. It is also known as a principal/primary/internal memory. | 2M |
| 1b) | An Instruction which specifies operation but not Address explicitly is referred as Zero-Address Instructions. For Example Take a expression A+B the code For A+B as Follows:  PUSH A  PUSH B  ADD  POP | 2M |
| 1c) | Performing 2’s Complement Arithematic Operation for the following equations:  (i) (+42) + (-13) and (ii) (-42) – (-13). | 2M |
| 1d) | The four basic operation supported by Instruction set are Data Tranfer, Arithematic, bit-wise and logic operations. | 2M |
| 1e) | Specifying Symbols for Registration Tranfer Language | 2M |
| 1f) | Control Memory is the storage in the microprogrammed control unit to store the microprogram. | 2M |
| 1g) | Virtual memory is a memory management technique where secondary memory can be used as if it were a part of the main memory. | 2M |
| 1h) | Any two differences between PROM and EPROM. | 2M |
| 1i) | Pipelining is the process of storing and prioritizing computer instructions that the processor executes. | 2M |
| 1j) | Explanatin briefly about Daisy chaining and Polling method | 2M |
|  | **PART-B** |  |
|  | **UNIT-1** |  |
| 2a) | Explanation about signed, 1’s Complement and 2’s Complement representations (1x3=3M)  Examples for the above Representations (1x2=2M) | 5M |
| 2b) | Block Diagram of the functional units of the Computer (2M)  Explanation of Each functioanl unit of a Computer (3M) | 5M |
|  | **OR** |  |
| 3a) | Any five differences between fixed and floating point representation like def, representation, scientific notations, examples of evaluation like adding, subracting etc. | 5M |
| 3b) | Multiplication Algorithm (Booth’s or Sign Magitude). (2M)  Division Algorithm (3M). | 5M |
|  | **UNIT-2** |  |
| 4a) | Register Classification like PC, MBR, MAR, IR and General Purpose Registers. (2M)  Puprose of Each Register. (3M) | 5M |
| 4b) | Direct, Indirect Register Addressing Modes Defintions(3M) with Examples. (2M) | 5M |
|  | **OR** |  |
| 5a) | Classification of Data Manipulation and Data Tranfer Instructions. (2M)  Explaining any three Data Manipultion and Tranfer Instruction with the Examples. (3M) | 5M |
| 5b) | Explanation about CISC Processors. | 5M |
|  | **UNIT-3** |  |
| 6a) | Any five Compartions between hardwired and microprogrammed control unit.(1X5=5M) | 5M |
| 6b) | Diagram for 4X1 Multiplexer (3M) | 5M |
|  | **(OR)** |  |
| 7a) | Arithemic Logical unit Circuit Diagram (3M)  Explaining the ALU operations with a state table (2M) | 5M |
| 7b) | Write any Microprogam examples like Fetch, Decode, Execute etc. (3M)  Explanation about the example (2M) | 5M |
|  | **UNIT-4** |  |
| 8a) | List Semiconductor Memories like RAM, ROM (1M)  Explanation about any Semiconductor Memory with a diagram (4M) | 5M |
| 8b) | Explantion about DMA working Principle (3M) with a Diagram (2M) | 5M |
|  | **(OR)** |  |
| 9a) | Explaining about Programmed IO working Principle (3M)  Issues related to Progammed IO (2M) | 5M |
| 9b) | Memory Hierarchy Diagram(2M) + Explanation about each role in the hierarchy. (3M) | 5M |
|  | **UINT-5** |  |
| 10a) | Arithematic Pipeline will improve the perforamace of the system during calculation(1M)  Pipe Line diagram for Addition and Substraction (3M) + Explanation(1M) | 5M |
| 10b) | Explanation about any InterProcess Arbitration System (2M) with Diagram(3M) | 5M |
|  | **(OR)** |  |
| 11a) | List interConnection Structures (1M)  Explain any two interconnection Structures with diagrams (2X2=4M) | 5M |
| 11b) | Explaination of 3 or 4 Segment RISC Pipeline Vector Processing with a suitable pipeline diagram | 5M |